Modeling and Characterization of Interconnects and IC Packages by FDTD 3D Simulation

Maynard Falconer and Vijai Tripathi
Electrical and Computer Engineering
Oregon State University
Corvallis, Oregon 97331-3211
falconm@ece.orst.edu Fax:(541)737-3598 Tel:(503)648-7117

ABSTRACT:

Time domain electromagnetic simulation of 3-D lossy interconnect coupling and ground bounce in a typical IC package is presented. The FDTD simulation tool is also proposed and used as a Virtual TDR (V-TDR) to extract the circuit models associated with complex 3D structures.

INTRODUCTION:

Power/ground bounce and coupling effects are becoming increasingly critical as integrated circuits continue to use smaller rail to rail voltage swings with faster risetimes. These same trends taken in conjunction with higher packing density of electronic package pins potentially lead to the additional problem of signal degradation and crosstalk. It is becoming increasingly important to select proper placement of the supply pins connecting the IC die power planes with the PCB power planes in order to minimize the ground bounce and crosstalk effects. Additionally it is important to have accurate circuit models when performing board level analysis and design. A lossy FDTD technique is applied to simulate and model power/ground currents and time domain responses including signal degradation and crosstalk in electronic packages.

The FDTD method gives the computed results for the electric and magnetic fields throughout the simulation space as a function of time[1]. By using a formulation applicable to general lossy media, the finite supply plane conductivities are included in the simulation allowing the observation of the current densities in the power/ground planes as a function of time. This paper includes examples of how the FDTD method for general lossy structures can be used to simulate and model power/ground bounce and crosstalk effects in IC packages. In addition, it is shown that the simulation can be used as a virtual time domain reflection/transmission (V-TDR) system to characterize complex coupled interconnect structures[2].

THEORY:

The well known FDTD method is a full wave simulation technique which uses a leap-frog approach to advance the fields through the simulation space as a function of time. To observe the current densities flowing through the ground planes and to simulate the effects of finite conductivities, a lossy FDTD formulation was employed. Berengers PML absorbing boundary conditions (ABCs) were implemented to reduce the demands on memory and CPU cycles[3]. The absorbing boundaries were validated against the Mur 1st and 2nd order ABCs using the methodology proposed by Moore[4-6].

The structure was excited by a vertical input plane between the IC ground plane and the IC pin to observe ground currents in the IC package. This corresponds to a negative voltage excitation for the interconnect. For the virtual TDR a 50[Ω] source with a Gaussian step function was used to excite the PCB traces.

Voltages are obtained by integrating the electric field, and current densities in the conducting planes are obtained by multiplying the electric field components by the corresponding conductivities.

RESULTS AND DISCUSION

Figure 1 shows the structure investigated to exemplify the lossy FDTD technique to simulate power/ground bounce and crosstalk. Here pins 1 and 4 are connected to the IC ground and the PCB ground planes. Pin 3 represents a passive interconnect and Pin 2 is excited by a 50[Ω] source between the PCB trace and the PCB ground plane. The IC package is assumed to be 1cm by 0.5cm with a ground plane which is 7.6mm by 3.8mm. The IC pins are 1mm wide, 0.3mm thick, and are separated by 1.2mm. The IC package is assumed to have a relative dielectric constant of 3 and the printed circuit board substrate is assumed to have a relative dielectric constant of 4. The conductivity of all metals is assumed to be 1e7(S/m).

Figure 3 shows the current densities in the IC ground plane at a single time step. The current densities can be viewed as a function of time using appropriate graphical software. Figures 2 and 4 show the crosstalk induced in the passive Pin 3 due to the proximity effects. Figure 2 is the vertical electric field component (Ey) in the X-Z plane directly under the PCB interconnects. Figure 4 is the voltage between the PCB interconnect and the PCB ground plane as a function of time as excited by the V-TDR. The impedance mismatch along the interconnect and at the input end lead to reflections in the waveforms shown in Figures 2 and 4.

Figure 5 shows the self and mutual admittance and impedance profiles associated with the characteristic admittance and impedance matrices of the nonuniform coupled interconnects. The profiles were obtained by applying a two dimensional peeling algorithm[7] to the V-TDR results in Figure 4. Multiple sections of three transmission lines, see Figure 6, can be used to create a SPICE equivalent circuit derived from the FDTD results. Figure 7 shows the comparison of the SPICE type circuit and the FDTD results. The deviations at the input of the circuit are due to the non-ideal source with insertion loss and the deviations at the end of the circuit are due to the non-ideal open inside the IC package. The system self- and mutual-equivalent inductances and capacitances can be obtained by integrating the admittance and impedance profiles with respect to time to obtain lumped inductor and capacitor type circuits [7].

A coupled microstrip structure whose time domain response derived from the FDTD simulation is shown in Figure 8. A 2.5[V] Gaussian pulse was chosen to excite the 4[mm] long structure to demonstrate the effects of dispersion and complex co- and contra-directional coupling in the coupled system, Figure 9. Again the simulation results can be used to extract the properties of the coupled system.

CONCLUSIONS

The FDTD method has been used as a V-TDR in conjunction with a two dimensional peeling algorithm to derive an equivalent SPICE type circuit for 3-D coupled interconnects. Simulation results for IC ground plane current density, coupling between lines, and radiation losses were also presented.

Use of FDTD simulations and it's application as a V-TDR allows the evaluation of package design options and other structures before prototyping. This should lead to cost and time reductions in a design cycle.

ACKNOWLEDGMENTS

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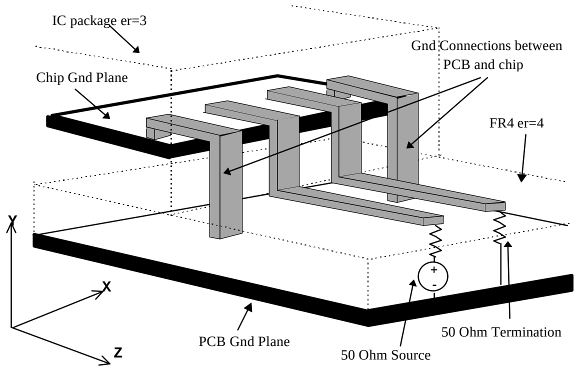

Figure 1 Simplified IC Package Test Structure

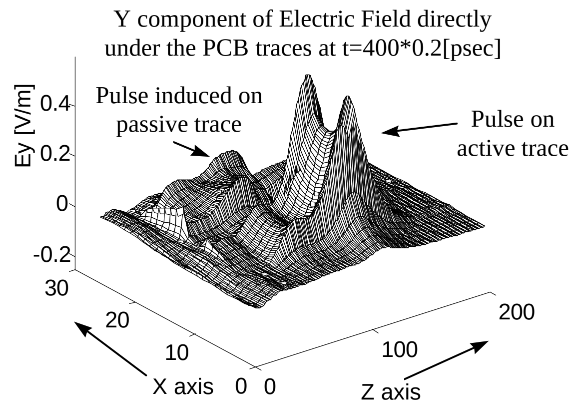

Figure 2 Electric Fields showing Crosstalk Effect

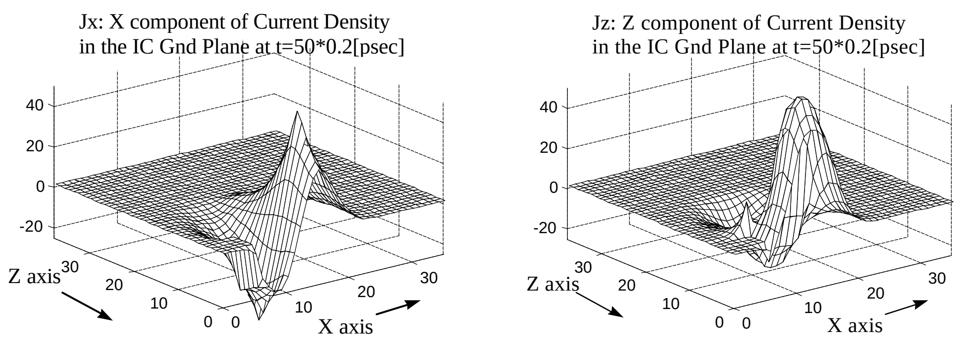

Figure 3 Current Density in IC Gnd Plane

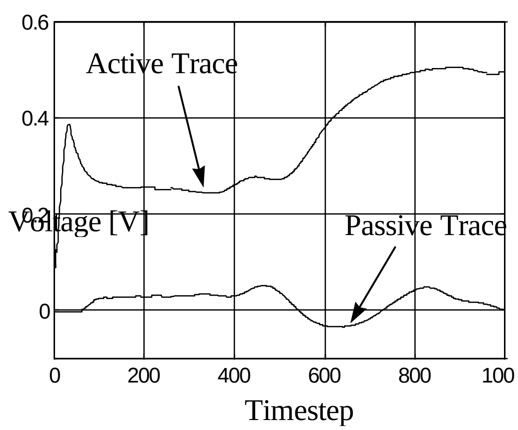

Figure 4 Virtual TDR Voltages of IC package

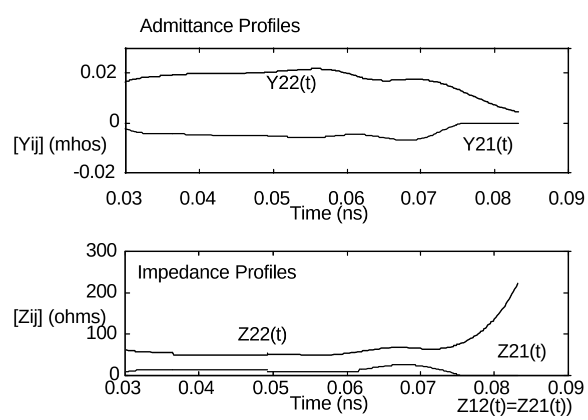

Figure 5 Admittance/Impedance Profiles of IC Package

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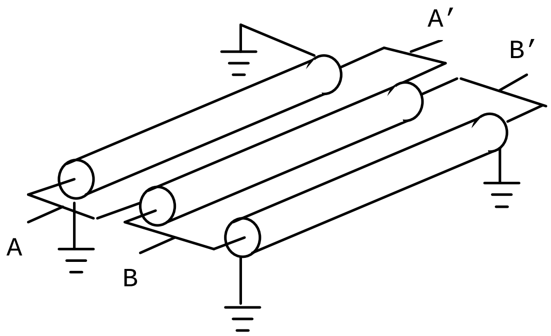

Figure 6 Transmission Line (SPICE) Model for each Piecewise Uniform Coupled Section

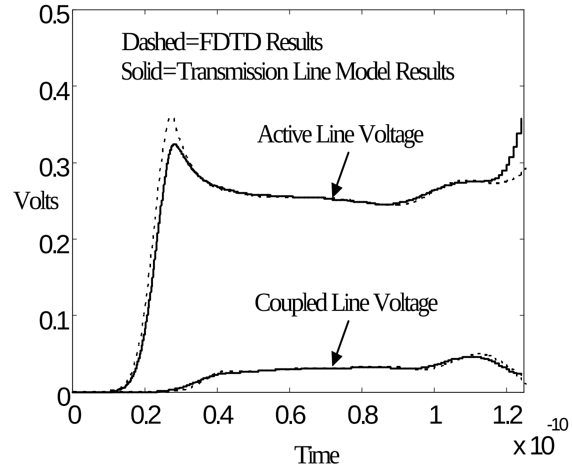

Figure 7 SPICE Simulation of Extracted Model and FDTD Results

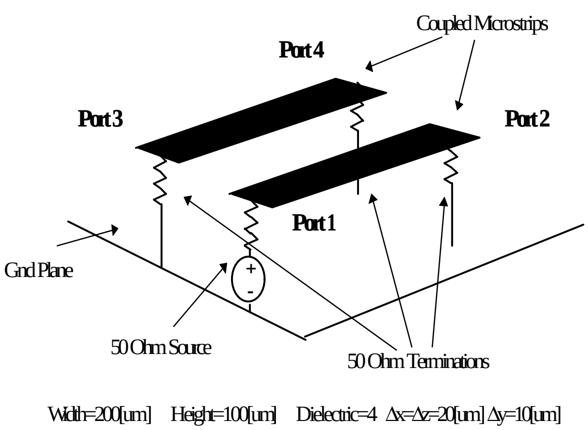

Figure 8 Coupled Microstrip Structure

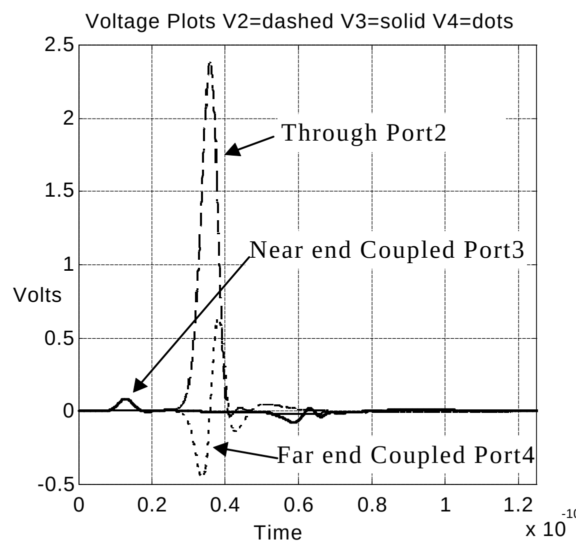

Figure 9 Coupled Microstrip Voltages

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